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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,549	08/02/2003	Marcos Karnezos	CPAC 1017-2	2569

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,549	KARNEZOS, MARCOS	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/05&5/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim1 is objected to because of the following informalities: in claim 1, line 5, second-level interconnection solder ball pads" should be changed to "interconnection solder ball pads". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma et al (US. 6,777,799) in view of Mori (US. 5,903,049).

Kikuma (Fig. 17B) discloses a multi-chip package module comprising stacked lower and upper die units, the upper die unit comprising an upper die 7A attached to and electrically interconnected to an upper die substrate 76 and the lower die unit comprising a lower die 72 attaches to and electrically interconnected to a lower die substrate 26, the module further comprising second-level interconnection solder ball pads (not labeled) at the lower side of the lower die substrate 26, wherein the electrical interconnections between each die and the substrate is protected, and wherein the upper and lower substrates are interconnected by wire bonding 86.

Kikuma does not disclose that the lower and upper dies 72/74 are encapsulated to form as the lower and upper packages.

However, Mori (Fig. 1) teaches the forming of a multi-package module comprising stacked lower and upper packages, the upper package 6a comprising an upper package die 1a attaches to an upper package substrate 2a and encapsulated by a sealing resin 5, and the lower package 6b comprising a lower package die 1b attaches to a lower package substrate 2b and encapsulated by a sealing resin 5, wherein the upper and lower substrates 2a/2b are interconnected by wire bonding 7. Accordingly, it would have been obvious to modify the multi-chip package module of Kikuma by encapsulating the lower die 72 and the upper die 74 with the sealing resins to form the lower and upper packages because such encapsulation would protect the lower and upper dies from the surrounding environment, as taught by Mori (column 2, lines 57-58).

Regarding claims 5-7, Kikuma (Fig. 17B) further discloses that the lower die unit is a ball grid array, and the upper die unit is a land grid array having flip chip interconnect of the die 74 with the substrate 76, and wherein the flip chip interconnect is protected by underfill (not labeled).

Regarding claim 10, it would have been obvious to add a third stacked package to the above multi-package structure because the number of the packages can be varied depending upon the required application for a multi-package module.

3. Claims 1-3, 5-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US. 5,903,049) in view of Lin (US. 5,222,014).

Regarding claims 1, 3 and 5, Mori (Fig. 1) discloses a multi-package module comprising stacked lower and upper packages, the upper package 6a comprising an upper package die 1a attached to and electrically interconnected to an upper package substrate 2a and the lower package 6b comprising a lower package die 1b attached to and electrically interconnected to a lower package substrate 2b, wherein the upper and lower packages 6a/6b are fully encapsulated by resin 5, and the upper and lower substrates 2a/2b are interconnected by wire bonding 7.

Mori does not disclose the interconnection solder ball pads at the lower side of the lower package substrate.

However, Lin (Fig. 6) teaches the forming of a multi-package module comprising stacked lower and upper packages, the upper package 44 comprising an upper package die 10 attaches to an upper package substrate 46 and the lower package 50 comprising a lower package die attaches to a lower package substrate 52, wherein the lower package substrate 52 has a plurality of interconnection solder ball pads 15 at the lower side. Accordingly, it would have been obvious to modify the multi-package module of Mori by forming the lower package 6b as a ball grid array (BGA) having the interconnection solder ball pads attached at the lower side of the lower package substrate 2b in order to mount the lower package 6b of the multi-package module to a PC board 8 by flip-chip bonding, as taught by Lin (column 4, lines 18-22).

Regarding claim 2, Lin (Fig. 6) further teaches the forming of the upper package 44 having wire bond interconnect 13 of the die 10 with the substrate 46 and wherein the wire bond interconnect 13 is protected by encapsulation 14.

Regarding claims 6-7, Mori (Fig. 1) further discloses that the upper package 6a is a land grid array package and has flip chip interconnect of the die 1a with the substrate 2a, wherein the flip chip interconnect is protected by an underfill 5.

Regarding claim 10, it would have been obvious to add a third stacked package to the multi-package structure of Mori because the number of the packages can be varied depending upon the required application for a multi-package module.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori and Lin as applied to claim 2 above, and further in view of LoBianco et al (US. 6,340,846)

The combination of Mori and Lin substantially reads on the above claim, including the upper package having wire bond interconnect of the die with the substrate. The above combination does not disclose that the package is encapsulated only to an extent.

However, LoBianco (Fig. 6) teaches a package has wire bond 38 interconnect of the die with the substrate 20, and the package is encapsulated by the adhesive 64 only to an extent. Accordingly, it would have been obvious to fully encapsulate or only partially encapsulate the upper package of the above combination because as taught by LoBianco, both encapsulations would provide the same results of protecting the wire bonds between the die and the substrate (column 5, lines 39-44).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma et al and Mori **or** Mori and Lin as applied to claim 1 above, and further in view of Barrow (US. 5,989,219).

The combination of Kikuma and Mori **or** Mori and Lin does not disclose a heat

spreader.

However, Barrow (Fig. 1) teaches the forming of a heat spreader 40 on a top surface of the package. Accordingly, it would have been obvious to form a heat spreader on a top surface of the multi-package module of the above combination because as taught by Barrow, such heat spreader would provide a thermal path, which can efficiently remove heat from the package module (column 2, lines 46-54).

6. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma et al and Mori **or** Mori and Lin as applied to claim 1 above, and further in view of Hoffman et al (US. 6,737,750).

Regarding claim 8, the combination of Kikuma and Mori **or** Mori and Lin does not disclose a heat spreader.

However, Hoffman (Fig. 1) teaches a stacked semiconductor packages having a heat spreader 14 (column 4, lines 50-52) formed on a top surface of a lower die 12a. Accordingly, it would have been obvious to form a heat spreader on a top surface of the lower package of the above combination because as taught by Hoffman, such heat spreader would provide a thermal path, which can efficiently remove heat from the package module (column 4, lines 50-52).

Regarding claim 9, the heat spreader 14 of Hoffman is inherently functioning as an electromagnetic shield because it is connected to a ground potential (column 6, lines 45-47).

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-3, 4-6 and 8-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 6-7, 13 and 19 of copending Application No. 10/632,552. Although the conflicting claims are not identical, they are not patentably distinct from each other because both instant application and copending application claim a semiconductor-package module having stacked second and first packages, each package including a die attached to a substrate, in which the first and second package substrates are interconnected by wire bonding, and in which the first package is a flip chip ball grid array package in a die0up configuration. Moreover, the claims in the instant application are either broader versions of the claims in copending application or are obvious variations thereof. For example, claim 1 in copending application claims "...the first package comprises a flip-chip ball grid array package having a flip-chip in a die-up configuration", whereas claim 1 in the instant application claims "...second-level interconnection solder ball pads at the lower side of the lower package substrate", that shows no different meaning between these two elements. The facts are that the claims of the instant application

and the copending application have claimed the same goal and are not distinguished from each other.

Response to Arguments

9. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

Because of the new issues presented in the amended claims, the new references are applied in the new ground of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 27, 2005

PHAT X. CAO
PRIMARY EXAMINER